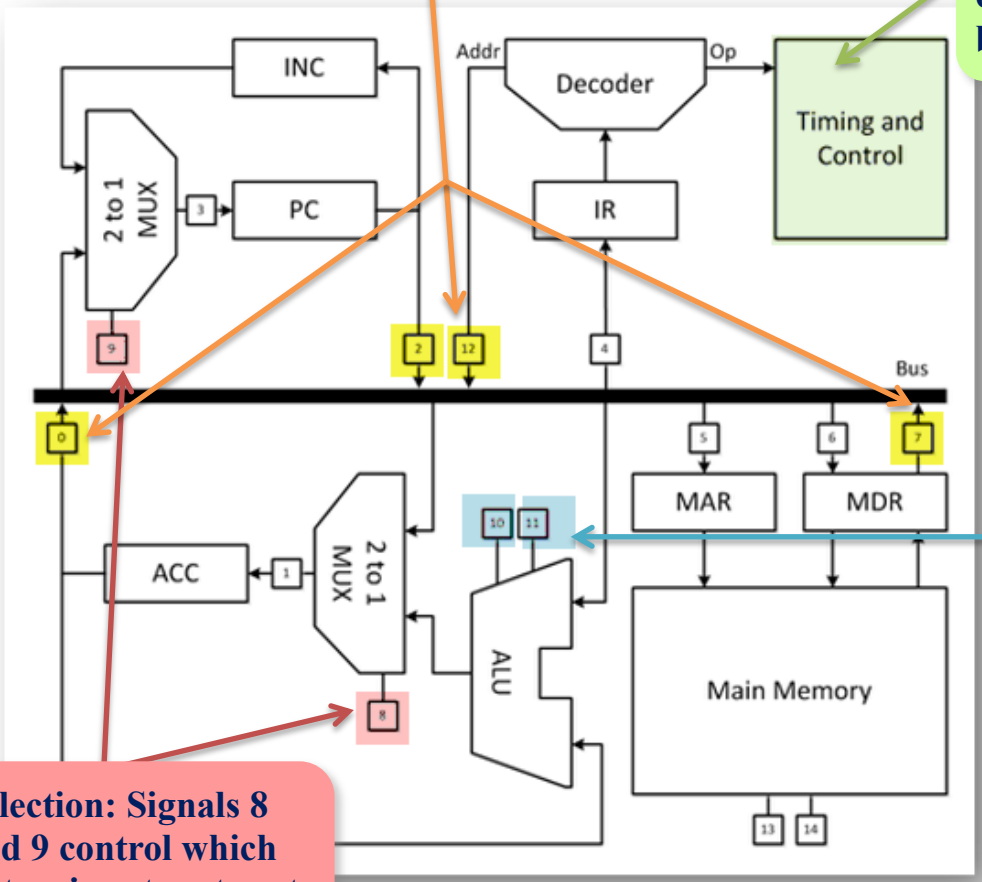
ملخص لمحتوى
شريحة رقم 5 في
Lecture 6
مع توضيح الأشياء التي ذكر الدكتور علي في
محاضرة قسم البنات أنهام مهمة

Fetch/Execute Cycle: Detailed Architecture

Bus Access: Signals 0, 2, 7, and 12 control which data gets written to the bus.

Control signals: determine order of operations, access to bus, loading of registers, etc.



ALU Operations: Signals 10 and 11 choose among addition, subtraction, multiplication and division performed by the ALU.

Selection: Signals 8 and 9 control which of two inputs get sent to output.

Number	Operation	Number	Operation
0	ACC→bus	8	ALU→ACC
1	Load ACC	9	INC→PC
2	PC→bus	10	ALU operation
3	Load PC	11	ALU operation
4	Load IR	12	Addr→bus
5	Load MAR	13	CS
6	Bus→MDR	14	R/W
7	Load MDR		

PC: Program Counter register, holds the address of the current Instruction being executed.

IR: Instruction Register, holds the actual instruction being executed currently by the computer.

MAR: Memory Address Register, holds the address of a memory location.

MDR: Memory Data Register, holds the address of a memory location.

Decoder: assembles the complete instruction with its operands, ready for execution